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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,002	02/25/2004	Herbert L. Ho	YOR920030635US1 (17343)	3930

23389 7590 01/25/2007
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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/787,002	HO ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on January 9, 2007.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1 and 13 each recite the limitation "...wherein said conductive back electrode is biased to form an inversion charge layer at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer which serves as an intrinsic collector of said transistor." The grammatical structure of the claims make it difficult to determine if back electrode, the inversion charge layer, or the first semiconductor layer and said insulating layer serve as an intrinsic collector of the transistor. For purposes of examination, the limitation will be interpreted in the following manner:

"...wherein said conductive back electrode is biased to form an inversion charge layer at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer, wherein the inversion charge layer serves as an intrinsic collector of said transistor."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miwa et al. (US 5,352,624) in view of Tsuchiya (JP 05-243255 A).

In re claims 1 and 13, Miwa shows (fig. 21E) bipolar transistor comprising: a conductive back electrode (603b) for receiving a bias voltage; a first semiconductor layer (550 in fig. 20E) located over said back electrode, said first semiconductor layer comprising a base which includes a first conductive type dopant (P) and an extrinsic collector (under COL region) which includes a second conductivity type dopant (N+), said extrinsic collector borders said base; and an emitter (under EM region) comprising a second semiconductor layer of the second conductivity type dopant (N+) located over a portion of said base. Miwa also shows at least one adjacent complementary metal oxide semiconductor device (MOS section II), wherein the bipolar transistor and the at least one adjacent complementary metal oxide device is separated by an isolation region (601). Miwa shows all of the elements of the claims except the insulating layer located over the conductive back electrode, the conductive back electrode located over a substrate layer, and conductive back electrode is biased to form an inversion charge layer in said base region at an interface between said first semiconductor layer and said insulating layer. Tsuchiya shows (fig. 1 and abstract) a bipolar transistor having a

conductive back electrode (12) for receiving a bias voltage and an insulating layer (13) located over the conductive back electrode. The bipolar transistor also comprises a semiconductor layer (11), wherein the conductive back electrode is located over the semiconductor substrate layer for receiving a bias voltage (V_{BG}). When combined, the inversion charge layer inherently serves as an intrinsic collector of the transistor because the structure and materials are the same as the applicant's claimed invention. With this configuration, a current amplification factor can be varied. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bipolar transistor of Miwa by adding an insulating layer between the back electrode and semiconductor layer as taught by Tsuchiya to vary the current amplification factor of the bipolar transistor.

In re claim 2, Miwa discloses (col. 42, lines 60-67) that a portion of said base is a doped to form an extrinsic base.

In re claims 3 and 4, Miwa discloses (col. 43, lines 15-22) that the base, the emitter, the extrinsic collector and the exposed surfaces of the conductive back electrode each include a silicided and the silicide is in contact with a metal contact that is located atop the silicide inside a contact opening formed in an interconnect dielectric.

In re claims 5 and 6, Miwa shows (fig. 21E) wherein the emitter comprises a single-finger (EM). In re the limitations concerning claim 6, Miwa does not show that the emitter has multi-fingers, however, It would have been obvious to one of ordinary skill in the art to use three, four, etc., emitter fingers since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See also MPEP 2144.04 VI. (B).

In re claim 7, Miwa shows (fig. 21E) that the extrinsic base (P) and collector (N+) are raised regions since they are formed in a semiconductor layer that is formed on top of the insulating layer (602).

In re claim 8, Miwa shows (fig. 21E) a spacer is located on the sidewalls of the emitter (603e).

In re claim 9, neither reference shows the range of thickness of the insulating layer, however it would have been obvious to one of ordinary skill in the art to make the thickness of the insulating layer within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

In re claim 10, Miwa shows (figs. 21B-21E) that another insulating layer (602) is located adjacent to the back electrode and said insulating layer is a buried oxide of an SOI. When combined with Tsuchiya, the another insulating layer (602) of Miwa would be thicker than the thin insulating layer and located adjacent thereto.

In re claim 11, Miwa shows (fig. 21E) that the base contains a p-type dopant, the emitter contains an n-type dopant, (N+ under EM region), and the extrinsic collector contains an n-type dopant (N+ region), and the extrinsic base contains a p-type dopant (col. 42, line 60 - col. 43, lines 11).

In re claim 12, Miwa shows (fig. 21E) that the extrinsic base (portion labeled P within the base region) diffuses minimally into the base so as not to be in contact with the underlying insulating layer (602 in fig 21B).

In re claim 14, Miwa shows (fig. 21E) that the complementary metal oxide semiconductor device is a field effect transistor because it is a MOSFET.

Response to Arguments

Applicant's arguments filed with respect to claims 1-14 have been fully considered but they are not persuasive. The applicant primarily asserts that the combined references do not show all of the elements of the claims, specifically that Miwa and Tsuchiya (JP' 255) do not disclose that the back gate forms an inversion charge layer during biasing. The examiner believes that the cited references show all of the elements of the claims and that Tsuchiya shows proper motivation for the combination. As stated in the rejection above, Tsuchiya was cited to cure the deficiencies of Miwa by disclosing a back gate electrode provided between the semiconductor layer and insulating layer to provide a bias. Tsuchiya specifically states in the CONSTITUTION portion of the Abstract that when "a back gate bias VBG are gradually raised from 0V, a thickness of a depleted layer 18 generated in a boundary between a p-type base region 16 and an SiO_2 film is increased, and hence a current amplification factor is increased." Although Tsuchiya does not call it an inversion layer, the depleted layer 18 (shown in fig. 1) is formed by the back gate biasing and is thus an

inversion layer. Tsuchiya even specifically states that the current amplification factor is increased in the transistor. Thus, Tsuchiya cures the deficiencies of Miwa and provides the motivation of increasing current amplification factor in the device. Although Tsuchiya does not specifically state that the inversion layer serves as an intrinsic collector, as stated in the rejection above, the inversion layer of Tsuchiya inherently serves as such since the materials and structure are the same as the applicant's claimed invention. Therefore, the cited references show all of the elements of the claims and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
January 22, 2007